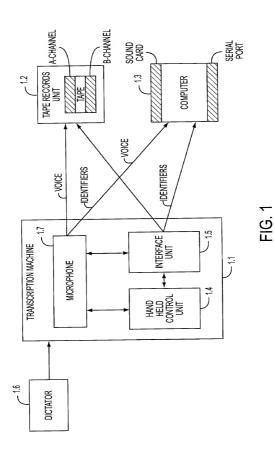
DOZNASAS "DEDIOI



Inventor: Krishnamurthy, et al. Appln. No.: 09/752,528 Ref. No.: Q61414 1 MASTER CLOCK **JUUUL** - 2.4 (4) (3) BAUD CLOCK X 64 CLK PROGRAMMABLE PULSE WIDTH **GENERATOR** CLK - 2.5 (5) 50-800 MS CLOCK BAUD STROBE **GENERATOR** (6) SELECTABLE BAUD 2400 TO 19200 CASCADED 8BIT COUNTER 2.107 2.7 (7) (10) RS232 LEVEL UART PARALLEL DATA CONTROL SERIAL OUT COM PORT (8) **ENCODING** LOGIC (9) START BIT & 16 BIT DATA SERIAL TRAIN HEAD ISOLATION CIRCUIT HEAD COIL OF TRACK

SEQUENTIAL-DATA SYNCHRONIZATION AT REAL-TIME ON AN ALALOG AND A

DIGITAL MEDIUM ,

FIG. 2

Inventor: Krishnamurthy, et Appln. No.: 09/752,528 Ref. No.: Q61414

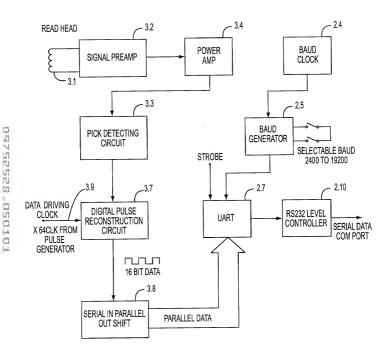


FIG. 3

CENTIAL-DATA SYNCHRONIZATION AT REAL-TIME ON AN ALALOG AND A DIGITAL MEDIUM Inventor: Krishnamurthy, et al. Appln. No.: 09/752,528 Ref. No.: 06/1414

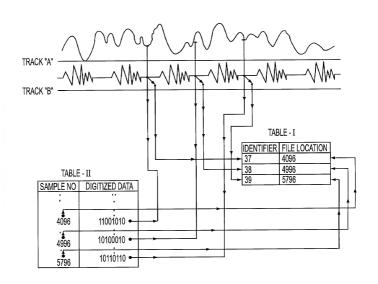


FIG. 4